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WHAT IS CLAIMED IS:

1. A bus controller that controls processing levels of plural requesters which access a common memory, including:

an access cycle counter for counting the number of access cycles for which the common memory is accessed;

a processing means for performing a processing of a processing level that is selected from plural processing levels that are different dependent on each requester;

a correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers;

a processing level judging means for indicating a processing level of the processing performed by the processing means of the respective requesters for which an access permission is given; and

said processing level judging means indicating the processing levels of the respective requesters for which an access permission is given, in accordance with a present cycle number that is counted by the access cycle counter, the number of remaining cycles up to a predetermined limit cycle number, and the correspondence information showing the correspondences between the processing levels of the respective requesters and the access cycle numbers.

2. A bus controller that arbitrates plural access requests

which are issued from plural requesters that would access a common memory, including:

an access cycle counter for counting the number of access cycles for which the common memory is accessed;

a correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers;

an arbiter that arbitrates the plural access requests which are issued from the plural requesters; and

said arbiter performing a control for giving no permission to a non-realtime bus access request when it is expected that a total number of cycles of all the requesters would exceed the limit cycle number in accordance with a present cycle number that is counted by the access cycle counter, the number of remaining cycles up to a predetermined limit cycle number, and the correspondence information that shows correspondences between the plural requesters and the access cycle numbers.

3. A bus controller that controls processing levels of plural requesters which access a common memory, and arbitrates plural access requests that are issued from the plural requesters, including:

an access cycle counter for counting the number of access cycles for which the common memory is accessed;

a processing means for performing a processing of a

processing level that is selected from plural processing levels which are different dependent on each requester;

a correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers;

a processing level judging means for indicating a processing level of the processing performed by the processing means of the respective requesters for which an access permission is given;

an arbiter for arbitrating the plural access requests which are issued from the plural requesters which would access the common memory, and

said processing level judging means and said arbiter indicating the levels of the processings which are performed by the processing means of the respective requesters for which an access permission is given, in accordance with a present cycle number counted by the access cycle counter, the number of remaining cycles up to a predetermined limit cycle number, and the correspondence information, and performing a control for giving no permission to a non-realtime bus access request when it is expected that a total number of cycles of all requesters would exceed the limit cycle number.

4. The bus controller of Claim 1 including:

the processing level judging means

calculating a total sum of the numbers of access cycles when

performing processings from a processing of a requester, which is two processings after a present one, to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

obtaining the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

selecting a processing level of a next processing of a requester within a range of the cycle number that is obtained by subtracting the total sum from the number of the remaining cycles.

5. The bus controller of Claim 2 including:

the arbiter

calculating a total sum of the numbers of access cycles when performing processings from a next processing of a non-realtime requester as a next requester to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

obtaining the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

performing a control for giving no permission to the non-realtime requester when the processings cannot be completed within a range of the cycle number that is obtained by subtracting the total sum from the number of remaining cycles.

6. The bus controller of Claim 3 including:

the processing level judging means and the arbiter calculating a total sum of the numbers of access cycles when performing processings from a next processing of a non-realtime requester as a next requester to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

obtaining the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

performing a control for giving no permission to the non-realtime requester when the processings cannot be completed within a range of the cycle number that is obtained by subtracting the total sum from the number of remaining cycles.

7. The bus controller of Claim 6 wherein

the non-realtime requester has plural different processing levels.